

### **In the Claims**

Claims 6, 8 through 11, 15 and 21 are pending in this application. Please cancel Claims 1 and 7 without prejudice or disclaimer, with Claims 2 through 5, 12 through 14 and 16 through 20 being previously cancelled without prejudice or disclaimer, and amend Claims 6, 8, 10, 11 and 21, as follows:

1.-5. (Cancelled)

6. (Currently Amended) The memory of Claim 8 [[1]], further comprising a latch connected to the write word line, wherein the latch is configured to hold a decoded write word line activation signal based on a previously decoded address to drive the paired read word line.

7. (Cancelled)

8. (Currently Amended) A memory, comprising:

a memory column including,

a plurality of word line pairs,

a pair of data lines, wherein the plurality of word line pairs intersects the pair of data lines at intersections, and

memory cells, wherein each memory cell is coupled to one of the plurality of word line pairs and the pair of data lines, wherein each of the plurality of word line pairs include a read word line and a write word line, and the read word line and the write word line which are included in different word line pairs can both be active simultaneously, The memory of Claim 7,

wherein the pair of data lines includes a read data line and a write data line,  
wherein the memory further comprises:

a latch having a latch input and a latch output, wherein the latch input  
is connected to the read data line and to an input data line, wherein the latch is  
configured to hold data of the input data line or data of a connected memory  
cell, wherein the latch output is connected to the write data line, and

wherein the memory column further comprises a sense amplifier configured to connect the read data line to the latch, wherein the read data line is connected to a sense amplifier input, wherein a sense amplifier output is connected to the latch input.

9. (Original) The memory of Claim 8, wherein when a same memory cell receives a consecutive read access, the memory is configured to read data held in a connected latch of the same memory cell and not data stored in the same memory cell.
10. (Currently Amended) The memory of Claim 8 [[1]], wherein at least one of the memory cells is one of:  
a three-transistor dynamic memory cell; or  
a three-transistor dynamic memory cell including a write transistor, wherein the write transistor is a thin-channel polysilicon transistor having a channel region thickness of 5 nanometers or less.
11. (Currently Amended) The memory of Claim [[7]] 8, wherein when a same memory cell receives a consecutive write access from an external input data bus, the latch stores data from the external input data without reading data from the memory cell.

12-14. (Cancelled)

15. (Original) The memory of Claim 8, further comprising another memory column configured like the memory column, wherein the memory column and the other memory column share the latch, wherein the memory is configured to conserve space on a silicon die in which the memory is fabricated due to sharing of the latch.

16-20. (Cancelled)

21. (Currently Amended) The memory of Claim 8 [[7]], wherein the latch stores data read out from one of the memory cell in a first cycle and outputs the data to the write data line in a second cycle and wherein another memory cell receives a read access in the second cycle.